A HIGHLY INTEGRATED RADIO TRANSCEIVER CHIPSET FOR DECT

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Abstract

A two chip solution for the DECT (Digital Enhanced Cordless Telecommunications) system has been implemented using Si bipolar technologies. A front end device implements up and down converting mixers, a VCO, driver amplifiers etc. using a high speed 24GHz NPN bipolar process. The IF device includes a down converting mixer, VCO, IF limiting strip with RSSI, on chip band-pass Gm-C filters and a fully integrated PLL demodulator. This device is implemented using a high speed complementary bipolar process. Both IC's include on-chip voltage regulation and power management.

Introduction

The access protocol defined by the DECT standard is intended to serve a number of high volume markets including domestic cordless telephony, wireless local loop (WLL) and wireless office systems (WPBX). The success of DECT in these markets will depend critically on the bill of material (BOM) cost for the radio. Secondary factors will include ease of manufacture, radio performance and battery life. This therefore requires the availability of highly integrated RF and IF ICs dedicated to the DECT requirements.

In this paper we describe a complete radio transceiver based around two such custom ICs. The RF IC implements a 1.9GHz down converting mixer and a corresponding up-conversion path including a PA driver. Also integrated is a VCO operating at 1.8GHz. This device consumes 34mA in Rx mode. The IF IC is a highly integrated device containing a down converting mixer, additional IF band-pass filtering, a limiting IF strip with successive detection logarithmic RSSI, a PLL demodulator, a VCO used for both Tx and Rx and baseband filters for shaping the received and transmitted data . This device consumes 24mA in Rx mode. These IC's have performance that exceeds the DECT requirements allowing a radio with -93dBm sensitivity (corresponding to a system NF of 8dB) to be implemented.

System Architecture

The major architectural decision for the receiver is whether to employ a single conversion or a dual conversion architecture. Comparisons of each approach have been made elsewhere e.g. [1], however the decision to use the dual conversion approach was based upon:

1. The SAW filtering requirements can be reduced at the 1st IF (1IF) by splitting the filtering between the 1IF and 2nd IF (2IF).
2. Simplified isolation requirements resulting in reduced risk
3. Improved manufacturability
4. Easier to achieve better sensitivity and overall dynamic range requirements.

A final ingredient in this decision process was that the program was part of a joint venture to supply components to a WLL program in India where time to market was critical. This decision was borne out in that it was possible to construct a complete operating DECT radio within 4 days of receiving the 1st silicon prototypes. The complete radio architecture is shown in Fig 1.

During Rx operation, the RF IC downconverts an 1880-1900MHz RF signal to a 110.592MHz 1st IF

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(IF1) while transmitting it upconverts a 131MHz IF to 1880-1900MHz. In Rx mode the IF transceiver downconverts to a 2nd IF (IF2) of 20.736MHz, and then filters and amplifies the signal. The band-pass filter centered at IF2 implements additional selectivity allowing the use of lower cost plastic packaged SAW filters at IF1. Along with the IF amplification, a RSSI (Received Signal Strength Indication) output with approximately 80dB of signal detection range is derived.

The limited output of the IF amplifiers is demodulated via a PLL, which uses a fully integrated VCO. The PLL contains two loops: one for rapid frequency acquisition and a second for demodulation. At a suitable time during the TDMA burst (e.g. during the 27μs inter-slot guardband) the frequency acquisition loop locks the VCO to a non-integer multiple of the system clock (either 3/2 or 5/2). Once locked, this loop voltage is stored on an external capacitor - which sets the initial VCO free running frequency prior to demodulation during which a 2nd loop is enabled. The demodulation PLL generates a baseband voltage at the loop filter proportional to the frequency deviation of the received signal. The PLL VCO and the IF2 band-pass filter are both constructed using matched Gm-C elements and therefore the frequency acquisition loop is also used to set the filter centre frequency by slaving it to the VCO. An active data filter is then used before presenting the output to a baseband controller that is used for timing recovery and data decision slicing.

During transmit mode, the IF transceiver implements a low-pass filter, that together with an appropriate input from a baseband ROM-DAC produces Gaussian-FSK (BT=0.5) via modulation of the 131MHz IF VCO. This signal is then up-converted to the final transmit by the RF IC and amplified to a level of +2dBm suitable for driving the external PA. An external dual synthesiser (one for synthesising the 1LO and one for the 2LO) is required to complete the radio implementation, along with an external LNA and PA.

RF IC

The RF IC has been described in detail elsewhere [2], but key features include
- on chip balun for single ended Tx drive
- 1.8GHz VCO which does not require band-switching for Rx/Tx
- single ended mixer input (class-AB input stage)
- simple to construct a zero-blind slot DECT radio

Key measured performance Results

SSB Phase Noise @ 4.7MHz	-136dBc/Hz
Rx Mixer Conversion Gain	16dB
SSB NF	17dB
IP3i / P1dBi	-5dBm/-12dBm
Tx Drive Level	+2dBm
Icc (Rx)	34mA
Icc(Tx)	56mA

IF IC

The majority of DECT IC implementations to date have used a FSK demodulator based on a passive external quadrature network (which performs frequency to phase conversion) followed by a phase detector. This has several drawbacks including (i) the requirement for some form of manufacturing set up and (ii) performance degradation in the presence of wideband noise due the non-linear nature of the phase detector. The use of a PLL demodulator gives FM threshold extension [3] and hence improved performance (when measured in terms of required C/N_i for a given S/N_o).

The on-chip band-pass filter is implemented using two coupled resonators synthesised using Gm-C elements [4]. The dynamic range of this filter is important since
(i) we are designing a low noise IF strip of which the filter is part
(ii) The filter must be reasonably linear to prevent intermodulation from adjacent channels and compression affecting the receiver performance. Furthermore, since it is the transconductance (Gm) that sets the filter center frequency, the compression point of the filter should be sufficiently large to prevent frequency pulling of the filter under large signal conditions.

Using a complementary bipolar process allows a transconductor that has fundamentally higher dynamic range than that possible on an all NPN technology (for a given topology and supply current). Consider the Gm stage shown in Fig. 2. This uses 2 offset long tailed pairs (with emitter

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areas in the ratio of 4:1) to linearize the "tanh" characteristic of a simple differential amplifier - this approach is sometimes called a multi-tanh doublet. The fundamental noise limit of this can be described by an equivalent input referred noise given by the collector shot noise divided by the stage transconductance. The Gm stage used in Fig. 3 is a simplified version of that used on the IC, where PNP and NPN stages are placed in parallel to obtain re-use of the bias current. This increases the Gm by a factor of 2x where the noise increases by $\sqrt{2}$. Therefore for the same bias current there is a net improvement in dynamic range by $\sqrt{2}$ or 3dB.

It is necessary for the o/p to be biased at a well defined d.c. voltage. This is achieved via a separate common mode feedback loop.

The PLL VCO uses a matched transconductance element. This gives a VCO gain that is dependent on both temperature and on-chip component values. A post PLL amplifier corrects the amplitude of the demodulated signal giving a demodulator gain independent of these effects. This gives a constant level to the ADC of a baseband processor operating a soft decision slicing algorithm.

Key IF Circuit Parameters

RSSI Range	-5dBm to -85dBm
3rd Adjacent channel rejection	20dB
Demodulator Gain	2.5V/MHz
C/Ni for 10^{-3} BER	12dB

Both the RF and IF IC contain low drop out voltage regulators that allow direct operation from a battery and ensure stable operating voltages for the RF circuitry. The VCOs are particularly sensitive to the transients that occur when the external PA is turned on for a transmit burst and the battery voltage abruptly drops. The IF IC uses an external low-cost PNP pass device and the IF IC an integrated vertical PNP transistor.

Measured results for the ICs are shown in Figs 4-6.

Technology

The RF IC was fabricated using ADRF a 22GHz Ft, double-polysilicon self-aligned silicon bipolar technology. Typical parameters are shown below (for a 0.8x5.0μm emitter):

Ft = 24GHz	Cbc =13fF	Cbc =13fF	Rbb′=200Ω

The IF IC was fabricated using XFCB a wafer bonded complementary bipolar process using trench isolation. Typical device electrical performance :

Ft (NPN) = 4GHz / Ft (PNP) = 2.5GHz
β(NPN) = 95 / β(PNP) = 75

This process also features high linearity Metal-oxide-Metal capacitors, trimmable thin film SiCr resistors and Schottky diodes.

Conclusion and Summary

A chipset for implementing a DECT radio has been presented based on an advanced high integration dual conversion architecture. The circuits can operate directly from NiCd batteries due to integrated supply regulation .The IF IC uses an advanced analog process to integrate a PLL demodulator and IF strip with on chip band pass filtering. Low cost dual in line packaging is used for both ICs. These devices are key components in future cordless phones and WLL systems.

Acknowledgements

The authors wish to thank J.M Mourant and G.Dawe for the RF IC design, M.Mendes and T.Murphy for taking the measurements, P.Brokaw for the regulator design, P.Katzin and Z.Zvonar for architecture and specification development and A.O'Rourke for programme management.

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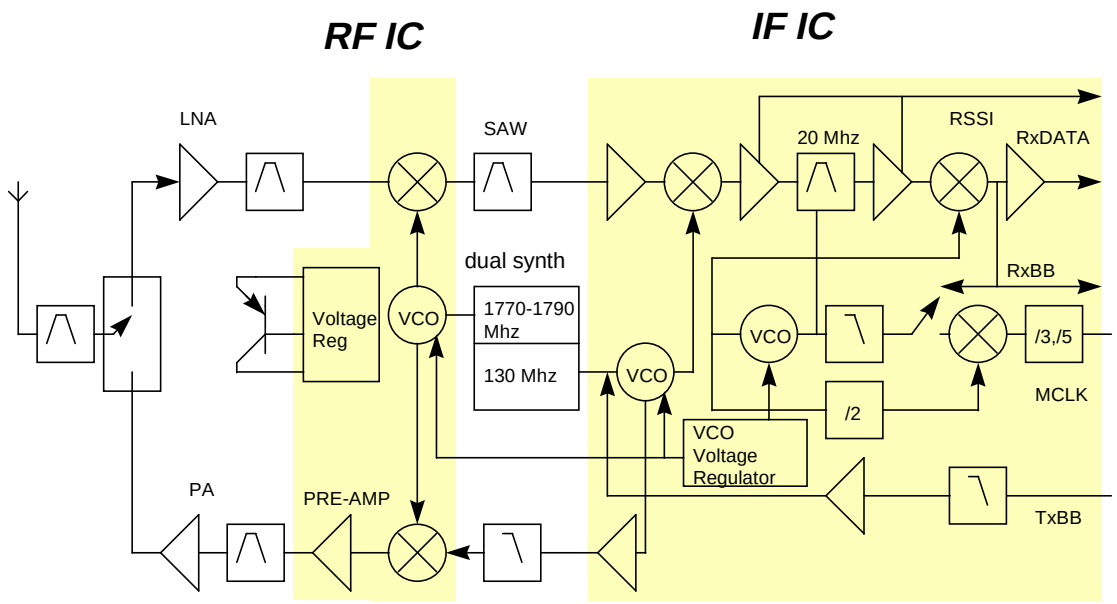

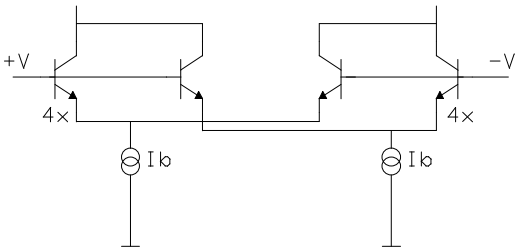

Figure 2: Conventional multi-tanh doublet

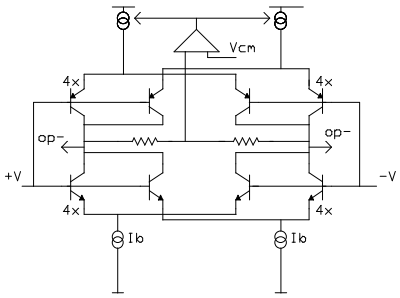

Figure 3: Complementary doublet

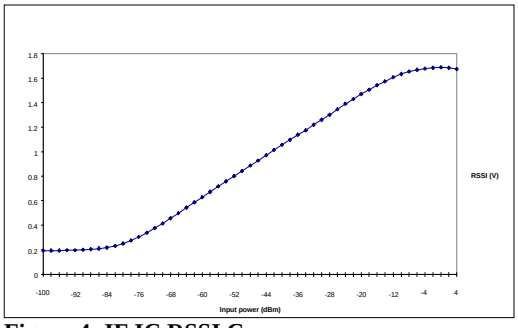

Figure 4: IF IC RSSI Curve

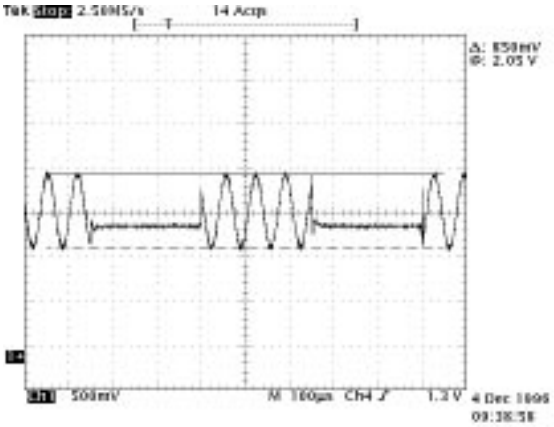

Figure 5: Demodulation via PLL

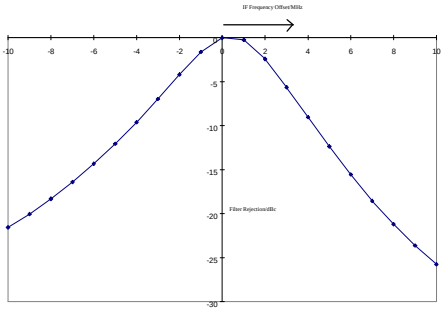

Figure 6: 2nd IF bandpass response